



Sierra Components, Inc.

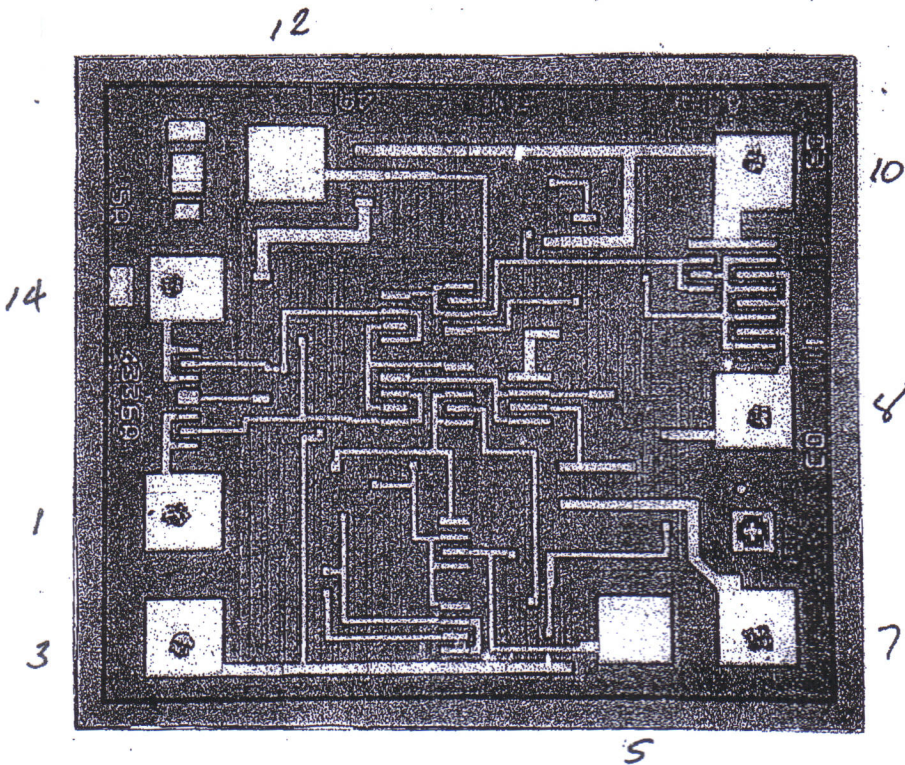
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Chip back potential is the level which bulk silicon is maintained by on-chip connection, or it is the level to which the chip back must be connected when specifically stated below. If no potential is given the chip back should be isolated.

Mfr. SIG Device SNE5539

FILE # SF-143-2



CONFIGURATION

SIZE 046 x 040

MASK# _____

PRELIM. PREP: 021

FINAL PREP: B27

PAD FUNCTIONS

- | | |
|---------------|------------------|
| 1) <u>+IN</u> | 10) <u>V+</u> |
| 2) <u>NC</u> | 11) <u>NC</u> |
| 3) <u>-V</u> | 12) <u>FILTR</u> |
| 4) <u>NC</u> | 13) <u>NC</u> |
| 5) <u>VDD</u> | 14) <u>-IN</u> |
| 6) <u>NC</u> | 15) _____ |
| 7) <u>GND</u> | 16) _____ |
| 8) <u>OUT</u> | 17) _____ |
| 9) <u>NC</u> | 18) _____ |

Topside Metal: Aluminum

Backside Metal: Silicon

Backside Potential:

Bond Pad Size: .004" Min.

Mask Ref:

MFG: Signetics (Philips)

THICKNESS: .021"

Part # NE5539

APPROVED BY: R Bacon

DIE SIZE : .040"x .046"

DATE: 5/13/09